12-11-6

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PTO/SB/21 (09-06)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

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Total Number of Pages in This Submission	

Application Number	10/799,244
Filing Date	MARCH 12, 2004
First Named Inventor	WARREN M. FARNWORTH ET AL.
Art Unit	2116
Examiner Name	TSE W. CHEN
Attorney Docket Number	MI22-2488

ENCLOSURES *(Check all that apply)*

- [✓] Fee Transmittal Form
  - [✓] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [✓] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [✓] Other Enclosure(s) (please Identify below):

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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	WELLS ST. JOHN P.S. (Customer No. 021567)		
Signature	D. Malhotra		
Printed name	DEEPAK MALHOTRA		
Date	Dec. 8, 2006	Reg. No.	33,560

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EV979438121

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Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2006

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
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Filing Date	MARCH 12, 2004
First Named Inventor	WARREN M. FARNWORTH ET AL.
Examiner Name	TSE W. CHEN
Art Unit	2116
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METHOD OF PAYMENT (check all that apply)

☑ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☑ Deposit Account Deposit Account Number: 23-0925 Deposit Account Name: WELLS ST. JOHN P.S.

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☑ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☑ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims		Extra Claims	Fee ($)		Fee Paid ($)
_____	- 20 or HP =	_____	x _____	=	_____

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims		Extra Claims	Fee ($)		Fee Paid ($)
_____	- 3 or HP =	_____	x _____	=	_____

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		Extra Sheets		Number of each additional 50 or fraction thereof	Fee ($)		Fee Paid ($)
_____	- 100 =	_____	/ 50 =	_____ (round **up** to a whole number)	x _____	=	_____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): APPEAL BRIEF FILING FEE	500.00

SUBMITTED BY

Signature	D. Malhotra	Registration No. (Attorney/Agent) 33,560	Telephone (509) 624-4276
Name (Print/Type)	DEEPAK MALHOTRA		Date Dec. 8, 2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

Application Serial No. 10/799,244
Confirmation No. 8217
Filing Date ..... March 12, 2004
Inventors ..... Warren M. Farnworth et al.
Assignee ..... Micron Technology, Inc.
Group Art Unit 2116
Examiner ..... Tse W. Chen
Attorney's Docket No. MI22-2488
Customer No. 021567
Title: Computer Including Installable and Removable Cards, Optical Interconnect Between Cards, and Method of Assembling a Computer

APPEAL BRIEF

To: Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

From: Deepak Malhotra (Tel. 509-624-4276; Fax 509-838-3424)
Wells St. John P.S.
601 W. First Avenue, Suite 1300
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Sir:

Appellant is appealing from the final rejection of claims 1-7 and 14-38 in an Office Action dated July 21, 2006. A check is enclosed to cover the fee specified under 37 C.F.R. § 41.20(b)(2).

Real Party In Interest

The real party in interest is Micron Technology, Inc.

Related Appeals and Interference

There are no other appeals which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

Status of Claims

Claims 1-7 and 14-38 are pending. Claims 1-7 and 14-38 stand rejected. The claims appealed are claims 1-7 and 14-38.

Status of Amendments

No amendments were filed subsequent to the Office Action of July 21, 2006.

Summary of Claimed Subject Matter

Some aspects, defined by claim 1, provide a system comprising a housing 12 (p.7,ln.12-13,Fig.1). The system comprises a circuit board 14 supported in the housing 12 (p.7,ln.13-14,Fig.1). The system further comprises a plurality of slot connectors 16, 18, 20, 22 supported on the circuit board 14 (p.7,ln.14-15,Fig.1). The system further comprises a first card 24 in one of the slot connectors 16, 18, 20, 22 (p.7,ln.15-17,Fig.1). The system further comprises a first circuit component 28 mounted on the first card 24 (p.7,ln.19-20,Fig.1). The slot connector couples the first circuit component 28 to a power supply 60 (p.11,ln.1-3,Fig.1). The system further comprises a second card 30 in another one of the slot connectors 16, 18, 20, 22 (p.7,ln.21-22,Fig.1); a second circuit component 40 mounted on the second card 30 (p.8,ln.11-12,Fig.2); and an optical interconnect 44 coupling the first

card 24 to the second card 30 (p.8,ln.19-20,Fig.2-4,6). The first circuit component 28 is configured to communicate with the second circuit component 40 via the optical interconnect 44 (p.8,ln.20-21) The optical interconnect 44 is entirely supported by the first and second cards, whereby the optical interconnect 44 does not pass through the slot connectors 16, 18, 20, 22 so that interference that could otherwise be caused by signals to and from the first circuit component is impeded (p.13,ln.23-p.14,ln.2,Fig.2-4,6).

Other aspects, defined by claim 14, provide a computer 10 comprising a housing 12 (p.7,ln.12-13,Fig.1). The computer further comprises a circuit board 14 supported in the housing 12 (p.7,ln.13-14,Fig.1). A plurality of connectors 16, 18, 20, 22 are supported on the circuit board 14 (p.7,ln.14-15,Fig.1). The computer further comprises a first card 24 in a first one of the connectors (p.7,ln.15-17,Fig.1); a processor 28 supported by the first card 24 (p.7,ln.19-20,Fig.1); and a second card 30 in a second one of the connectors (p.7,ln.21-22,Fig.1). The computer further comprises a synchronous link DRAM memory supported by the second card 30 (p.8,ln.11-14,Fig.2); a power supply in the housing 12 (p.11,ln.1-2,Fig.1); and conductors coupling the power supply to the processor 28 via the first connector (p.11,ln.1-3,Fig.1). The conductors include circuit traces 62 on the first card 24 (p.11,ln.3-5). The conductors couple the power supply to the memory via the second connector (p.8,ln.20-21). The conductors include circuit traces on the second card 30 (p.11,ln.8-10); and an optical interconnect 44 coupling the processor to the memory for data communications (p.8,ln.19-22,Fig.2-4,6). The optical interconnect 44 is within the housing 12, in use, wherein the optical interconnect 44 does not pass through the connectors (Fig.2-4,6).

Other aspects of the invention, defined by claim 19, provide a computer 10 comprising a housing 12 (p.7,ln.12-13,Fig.1). A circuit board 14 is supported in the housing 12 (p.7,ln.13-14,Fig.1). A plurality of connectors 16, 18, 20, 22 are supported on the circuit board 14 (p.7,ln.14-15,Fig.1). A first card 24 is in a first one of the connectors 16, 18, 20, 22 (p.7,ln.15-17,Fig.1) . A first integrated circuit 28 is supported by the first card 24 (p.7,ln.19-20,Fig.1). A second card 30 is in a second one of the connectors (p.7,ln.21-22,Fig.1). A second integrated circuit is supported by the second card 30 (p.8,ln.11-14,Fig.2). A power supply 60 is in the housing 12 (p.11,ln.1-2,Fig.1). Conductors couple the power supply 60 to the first integrated circuit via the first connector, the conductors including circuit traces on the first card 24 (p.11,ln.1-5,Fig.1). Conductors couple the power supply 60 to the second integrated circuit via the second connector, the conductors including circuit traces on the second card 30 (p.11,ln.6-10,Fig.1). An optical interconnect 44 couples the first integrated circuit to the second integrated circuit for data communications (p.8,ln.20-24), the optical interconnect 44 being within the housing 12, in use, wherein the optical interconnect 44 does not pass through the connectors (p.8,ln.19-20,Fig.2-4,6).

Other aspects of the invention, defined by claim 24, provide a method of assembling a system. The method comprises supporting a circuit board 14 in a housing 12 (p.7,ln.12-13,Fig.1). The method further comprises supporting a plurality of slot connectors 16, 18, 20, 22 on the circuit board 14 (p.7,ln.14-15,Fig.1); mounting a first circuit component 28 on a first card 24 (p.7,ln.12-13,Fig.1); inserting the first card 24 into a first one of the slot connectors 16, 18, 20, 22 (p.7,ln.18-19); mounting a second circuit component on a second card 30 (p.8,ln.11-14,Fig.2); inserting the second card 30 into a second one of the

slot connectors 16, 18, 20, 22 (p.7,ln.21-22,Fig.1); and flexibly optically coupling the first card 24 to the second card 30 for optical communications between the first circuit component and the second circuit component (p.8,ln.20-24), using a first optical connector supported by the first card 24 and completely movable with the first card 24 (p.9,ln.5-9,Fig.1), a second optical connector supported by the second card 30 and completely movable with the second card 30 (p.9,ln.5-9,Fig.4), and an optical cable 46 coupled between the first and second optical connectors (p.8,ln.19-20,p.9,ln.4-5,Fig.2-4,6), whereby the flexible optical interconnect 44 does not pass through the slot connectors 16, 18, 20, 22 so that interference that could otherwise be caused by signals to and from the first circuit component is impeded (p.13,ln.23-p.14,ln.2,Fig.2-4,6).

Other aspects, defined by claim 31, provide a method comprising supporting a circuit board 14 in a housing 12 (p.7,ln.12-13,Fig.1); supporting a plurality of slot connectors 16, 18, 20, 22 on the circuit board 14 (p.7,ln.14-15,Fig.1); supporting a processor on a first card 24 having an edge connector (p.7,ln.19-20,Fig.1); inserting the edge connector of the first card 24 into a first one of the slot connectors 16, 18, 20, 22 to support the first card 24 from the circuit board 14 (p.7,ln.18-19,Fig.1); providing a second card 30 having an edge connector configured for sliding receipt in a second one of the slot connectors 16, 18, 20, 22; supporting a synchronous link DRAM memory on a second card 30 having an edge connector (p.8,ln.11-14,Fig.2); inserting the edge connector of the second card 30 into a second one of the slot connectors 16, 18, 20, 22 to support the second card 30 from the circuit board 14 (p.7,ln.21-22,Fig.1); supporting a power supply in the housing 12 (p.11,ln.1-2,Fig.1); coupling the power supply to the processor via the first slot connector, the coupling including using circuit traces on the first card 24 extending

from the edge connector of the first card 24 toward the processor 28 (p.11,ln.1-6); coupling the power supply to the memory via the second slot connector , the coupling including using circuit traces on the second card 30 extending from the edge connector of the second card 30 toward the memory (p.11,ln.7-10); and optically coupling the processor to the memory for data communications using an optical interconnect 44 within the housing 12 (p.8,ln.20-24), wherein the optical interconnect 44 does not pass through the slot connectors 16, 18, 20, 22 (p.8,ln.19-20,Fig.2-4,6).

Other aspects, defined by claim 35, provide a method comprising supporting a circuit board 14 in a housing 12 (p.7,ln.14-15,Fig.1); supporting a plurality of slot connectors 16, 18, 20, 22 on the circuit board 14 (p.7,ln.14-15,Fig.1); supporting a first integrated circuit on a first card 24 having an edge connector (p.7,ln.18-20,Fig.1); inserting the edge connector of the first card 24 into a first one of the slot connectors 16, 18, 20, 22 to support the first card 24 from the circuit board 14 (p.7,ln.18-20,Fig.1); providing a second card 30 having an edge connector configured for sliding receipt in a second one of the slot connectors 16, 18, 20, 22 (p.7,ln.21-22,Fig.1); supporting a second integrated circuit 40 on a second card 30 having an edge connector (p.8,ln.11-14,Fig.2); inserting the edge connector of the second card 30 into a second one of the slot connectors 16, 18, 20, 22 to support the second card 30 from the circuit board 14 (p.7,ln.21-22,Fig.1); supporting a power supply in the housing 12 (p.11,ln.1-2,Fig.1); coupling the power supply to the first integrated circuit via the first slot connector, the coupling including using circuit traces on the first card 24 extending from the edge connector of the first card 24 toward the first integrated circuit (p.11,ln.1-5,Fig.1); coupling the power supply to the second integrated circuit via the second slot connector, the coupling including using circuit traces on the

second card 30 extending from the edge connector of the second card 30 toward the second integrated circuit (p.11,ln.6-10,Fig.1); and optically coupling the first integrated circuit to the second integrated circuit for data communications using an optical interconnect 44 within the housing 12 (p.8,ln.20-24,Fig.2-4,6), wherein the optical interconnect 44 does not pass through the slot connectors 16, 18, 20, 22 (p.8,ln.19-20,Fig.2-4,6).

Grounds of Rejection to be Reviewed on Appeal

1. Whether or not claims 1-5 and 24-28 are patentable under 35 U.S.C. §103(a) over U.S. Patent No. 4,863,232 to Kwa, in view of U.S. Patent No. 5,631,988 to Swirhun et al. and U.S. Patent No. 4,704,599 to Kimmel et al.

2. Whether or not claims 6-7 are patentable under 35 U.S.C.§103(a) over Kwa, Swirhun et al., Kimmel et al. and Gillingham article titled "SLDRAM: High-Performance, Open-Standard Memory."

3. Whether or not claims 14-16, 18-21, 23, 31-33 and 35-37 are patentable under 35 U.S.C.§103(a) over Kwa in view of Kimmel et al. and Gillingham.

4. Whether or not claims 17, 22, 34 and 38 are patentable under 35 U.S.C.§103(a) over Kimmel et al., Gillingham, Kwa, and U.S. Patent No. 4,839,829 to Freedman.

5. Whether or not claims 24-28 are patentable under 35 U.S.C.§103(a) over Kwa, in view of Swirhun et al.

6. Whether or not claims 29-30 are patentable under 35 U.S.C.§103(a) over Kwa, Swirhun et al., Kimmel et al., and Gillingham

Argument

Issue 1

Claims 1-5, and 24-28 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 4,863,232 to Kwa, in view of U.S. Patent No. 5,631,988 to Swirhun et al. and U.S. Patent No. 4,704,599 to Kimmel et al.

Claim 1 recites a system comprising a housing; a circuit board supported in the housing; a plurality of slot connectors supported on the circuit board; a first card in one of the slot connectors; a first circuit component mounted on the first card, the slot connector coupling the first circuit component to a power supply; a second card in another one of the slot connectors; a second circuit component mounted on the second card; and an optical interconnect coupling the first card to the second card, the first circuit component being configured to communicate with the second circuit component via the optical interconnect, the optical interconnect being entirely supported by the first and second cards, whereby the optical interconnect does not pass through the slot connectors so that interference that could otherwise be caused by signals to and from the first circuit component is impeded.

The Kwa reference fails to disclose an optical interconnect being entirely supported by the first and second cards. The Office Action states that Swirhun et al. discloses, in Fig. 4a, an optical interconnect coupling a first card 400 to a

second card 410, the first component being configured to communicate with the second circuit component via the optical interconnect, the optical interconnect being entirely supported by the first and second cards. The Examiner is taking the position that it would have been obvious to modify Kwa to include the teachings of Swirhun et al. and Kimmel et al. The stated motivation is that this would be a way to alleviate misalignment problems due to thermal strain.

If Kwa was modified with the arrangement of Fig. 4a of Swirhun et al., it would not be possible to use the slot connector to couple the first circuit component to a power supply. The slot connector of Fig. 4a of Swirhun et al. is not usable when the optical interconnect is being used.

Further, Kwa teaches away from any such combination. The main purpose of Kwa is to avoid the risk of operators forgetting to mate optical connector parts when inserting a circuit board or of forgetting to unmate optical connector parts when removing a circuit board by providing card guides 112. Therefore, Kwa would not have any system other than one that provides for automatic alignment of optical connector parts. Kwa would only have a system where the optical interconnects are not supported by the first and second cards. Otherwise there is no point to Kwa's invention.

Kwa states in Col. 1, lines 45 to 60 (in discussing problems with the prior art) that:

> Most optical connector parts are provided with screw or bayonet type fittings. Thus, tee optical connector parts must be rotatably mated after the circuit boards are inserted and rotatably unmated before the circuit boards are withdrawn. The optical connector parts must be mounted where they are manually

> accessible when the circuit boards are mounted in the frame, for example at the front of the frame. This is not always convenient or possible, particularly when the frame carries a large number of densely packed circuit boards. Moreover, operators may forget to rotatably mate the optical connector parts when inserting a circuit board, leaving the circuit board optically disconnected, or may forget to rotatably unmate the optical connector parts when removing a circuit board, physically damaging the circuit board, connector parts or optical fibers.

Kwa then goes on to state in Col. 2, lines 4 to 16 (in discussing problems with the prior art) that:

> Unfortunately, in the known board edge optical connector arrangements the circuit board mounted optical connector parts are mounted at leading edges of the circuit boards. These leading edges are already congested with board edge electrical contacts. Moreover, in the known board edge optical connector arrangements the frame mounted optical connector parts are mounted at the back plane which is already congested with electrical board edge connectors and electrical conductors.
>
> The present invention provides an optical connector which can be used to avoid some or all of the problems described above.

Kwa solves the problem of risk of operators forgetting to mate optical connector parts when inserting a circuit board or of forgetting to unmate optical connector parts when removing a circuit board by providing card guides 112 such that (see Col. 4, lines 8 to 44) sliding insertion of the circuit boards 140 into the card guides 112 urges the board edge electrical contacts 142 into the board edge electrical connectors 116 to electrically interconnect the circuit boards, and align the optical connector parts 120, 150 in a direction transverse to the direction of insertion.

Thus, Kwa itself teaches away from a system that does not provide for automatic alignment of optical connector parts. The main purpose of Kwa is to avoid the risk of operators forgetting to mate optical connector parts when inserting a circuit board or of forgetting to unmate optical connector parts when removing a circuit board by providing card guides 112. Therefore, Kwa teaches away from a combination with Swirhun et al. and Kimmel et al. The combination of references is improper and the rejection should be withdrawn.

In addition, the problem of alleviating misalignment problems due to thermal strain would appear to be solved by Swirhun et al. alone, without any need to look to Kwa's invention or Kimmel et al. Further, insufficient evidence has been presented to support motivation to combine the teachings of Kwa with Swirhun et al. and Kimmel.

Therefore, the combination of references is improper and claims 1-5 are allowable.

Claim 24 recites inserting the first card into a first one of the slot connectors.

If Swirhun et al. were combined with Kwa, it would not be possible to insert the first card into a first one of the slot connectors. The position of the optical connector in Fig. 4a of Swirhun et al. prevents use of the slot connector. Swirhun et al. does not disclose simultaneous use of an edge connector and an optical connector.

Therefore, claim 24 is allowable. As claims 25-28 depend on claim 24, they too are allowable.

Issue 2

Claims 6-7 stand rejected under 35 U.S.C.§103(a) as being unpatentable over Kwa, Swirhun et al., Kimmel et al. and the publication by Gillingham titled "SLDRAM: High-Performance Open-Standard Memory" (hereinafter referred to as "Gillingham").

This rejection is improper because Kwa teaches away with such a combination, for the reasons described above.

Further, this combination of four references is implausible absent improper hindsight reconstruction. Appellants assert that the Office's conclusion of obviousness is based on improper hindsight reasoning.

Issue 3

Claims 14-16, 18-21, 23, 31-33 and 35-37 stand rejected under 35 U.S.C.§103(a) as being unpatentable over Kwa in view of Kimmel et al. and Gillingham.

Claim 14 recites, in part, conductors coupling the power supply to the processor via the first connector, the conductors including circuit traces on the first card; and conductors coupling the power supply to the memory via the second connector, the conductors including circuit traces on the second card.

If Swirhun et al. were combined with Kwa, it would not be possible to use the first connector to couple the power supply to the processor. The connector of Swirhun et al. is intended to be used instead of the edge connector.

Therefore, claim 14 is allowable. As claims 15-16 and 18 depend on claim 14, they too are allowable.

Claim 19 recites, in part, conductors coupling the power supply to the first integrated circuit via the first connector, the conductors including circuit traces on the first card; and conductors coupling the power supply to the second integrated circuit via the second connector, the conductors including circuit traces on the second card.

If Swirhun et al. were combined with Kwa, it would not be possible to use the first connector to couple the power supply to the processor. The connector of Swirhun et al. is intended to be used instead of the edge connector.

Therefore, claim 19 is allowable. As claims 20-21 and 23 depend on claim 19, they too are allowable.

Claim 31 recites a method comprising supporting a circuit board in a housing; supporting a plurality of slot connectors on the circuit board; supporting a processor on a first card having an edge connector; inserting the edge connector of the first card into a first one of the slot connectors to support the first card from the circuit board; providing a second card having an edge connector configured for sliding receipt in a second one of the slot connectors; supporting a synchronous link DRAM memory on a second card having an edge connector; inserting the edge connector of the second card into a second one of the slot connectors to support the second card from the circuit board; supporting a power supply in the housing; coupling the power supply to the processor via the first slot connector, the coupling including using circuit traces on the first card extending from the edge connector of the first card toward the processor; coupling the power supply to the memory via the second slot connector, the coupling including using circuit traces on the

second card extending from the edge connector of the second card toward the memory; and optically coupling the processor to the memory for data communications using an optical interconnect within the housing, wherein the optical interconnect does not pass through the slot connectors.

The cited references, even if they could be combined, would fail to meet all the limitations of this claim.

If Swirhun et al. were combined with Kwa, it would not be possible to insert the first card into a first one of the slot connectors. The position of the optical connector in Fig. 4a of Swirhun et al. prevents use of the slot connector. Swirhun et al. does not disclose simultaneous use of an edge connector and an optical connector.

Therefore, claim 31 is allowable. As claims 32-33 depend on claim 31, they too are allowable.

Claim 35 recites, in part, inserting the edge connector of the first card into a first one of the slot connectors to support the first card from the circuit board.

If Swirhun et al. were combined with Kwa, it would not be possible to insert the first card into a first one of the slot connectors. The position of the optical connector in Fig. 4a of Swirhun et al. prevents use of the slot connector. Swirhun et al. does not disclose simultaneous use of an edge connector and an optical connector.

Therefore, claim 35 is allowable. As claims 36-37 depend on claim 35, they too are allowable.

Issue 4

Claims 17, 22, 34 and 38 stand rejected under 35 U.S.C.§103(a) as being unpatentable over Kimmel et al., Gillingham, Kwa, and U.S. Patent No. 4,839,829 to Freedman.

The rejection is improper because Kwa teaches away from any such combination.

Further, this combination of four references is implausible absent improper hindsight reconstruction. Appellants assert that the Office's conclusion of obviousness is based on improper hindsight reasoning.

Issue 5

Claims 24-28 stand rejected under 35 U.S.C.§103(a) as being unpatentable over Kwa, in view of Swirhun et al.

Claim 24 recites inserting the first card into a first one of the slot connectors.

If Swirhun et al. were combined with Kwa, it would not be possible to insert the first card into a first one of the slot connectors. The position of the optical connector in Fig. 4a of Swirhun et al. prevents use of the slot connector. Swirhun et al. does not disclose simultaneous use of an edge connector and an optical connector.

Therefore, claim 24 is allowable. As claims 25-28 depend on claim 24, they too are allowable.

Issue 6

Claims 29-30 stand rejected under 35 U.S.C.§103(a) as being unpatentable over Kwa, Swirhun et al., Kimmel et al., and Gillingham.

The rejection is improper because Kwa teaches away from any such combination.

In view of the foregoing, reversal of the rejections of claims 1-7 and 14-38 is requested.

Respectfully submitted,

Dated: Dec. 8, 2006 By: D. Malhotra

Deepak Malhotra, Reg. No. 33,560
Wells St. John P.S.

Customer No. 021567

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

Application Serial No. 10/799,244
Confirmation No. 8217
Filing Date .....March 12, 2004
Inventors .....Warren M. Farnworth et al.
Assignee .....Micron Technology, Inc.
Group Art Unit 2116
Examiner .....Tse W. Chen
Attorney's Docket No. MI22-2488
Customer No. 021567
Title: Computer Including Installable and Removable Cards, Optical Interconnect Between Cards, and Method of Assembling a Computer

Claims Appendix

The claims involved in the appeal are as follows:

1. A system comprising:

a housing;

a circuit board supported in the housing;

a plurality of slot connectors supported on the circuit board;

a first card in one of the slot connectors;

a first circuit component mounted on the first card, the slot connector coupling the first circuit component to a power supply;

a second card in another one of the slot connectors;

a second circuit component mounted on the second card; and

an optical interconnect coupling the first card to the second card, the first circuit component being configured to communicate with the second circuit component via the optical interconnect, the optical interconnect being entirely supported by the first and second cards, whereby the optical interconnect does not pass through the slot connectors so that interference that could otherwise be caused by signals to and from the first circuit component is impeded.

2. A system in accordance with claim 1 wherein the optical interconnect comprises a fiber optic cable.

3. A system in accordance with claim 1 wherein the optical interconnect comprises an optical connector on the first card configured to convert between electrical signals and optical signals, and wherein the system further includes circuit traces on the first card coupling the optical connector to the first circuit component.

4. A system in accordance with claim 1 wherein the optical interconnect comprises an optical connector on the second card configured to convert between electrical signals and optical signals, and wherein the system further includes circuit traces on the second card coupling the optical connector to the second circuit component.

5. A system in accordance with claim 1 wherein the optical interconnect comprises a first optical connector, on the first card, configured to convert between electrical signals and optical signals, wherein the system further includes circuit traces on the first card coupling the first optical connector to the first circuit component, wherein the optical interconnect further comprises an optical connector, on the second card, configured to convert between electrical signals and optical signals, the system further including circuit traces on the second card coupling the second optical connector to the second circuit component.

6. A system in accordance with claim 1 wherein the second circuit component comprises a DRAM.

7. A system in accordance with claim 1 wherein the second circuit component comprises a synchronous link type DRAM.

14. A computer comprising:

a housing;

a circuit board supported in the housing;

a plurality of connectors supported on the circuit board;

a first card in a first one of the connectors;

a processor supported by the first card;

a second card in a second one of the connectors;

a synchronous link DRAM memory supported by the second card;

a power supply in the housing;

conductors coupling the power supply to the processor via the first connector, the conductors including circuit traces on the first card;

conductors coupling the power supply to the memory via the second connector, the conductors including circuit traces on the second card; and

an optical interconnect coupling the processor to the memory for data communications, the optical interconnect being within the housing, in use, wherein the optical interconnect does not pass through the connectors.

15. A computer in accordance with claim 14 and further comprising a third card in a third one of the connectors, a co-processor supported by the third card, and an optical interconnect coupling the co-processor to the processor.

16. A computer in accordance with claim 15 and further comprising conductors coupling the power supply to the co-processor via the third connector, the conductors including circuit traces on the third card.

17. A computer in accordance with claim 15 wherein the co-processor is a math co-processor.

18. A computer in accordance with claim 15 and further including an electronic device in the housing capable of generating electromagnetic interference, and wherein the optical interconnect shields communications between the processor and the memory from the electromagnetic interference.

19. A computer comprising:

a housing;

a circuit board supported in the housing;

a plurality of connectors supported on the circuit board;

a first card in a first one of the connectors;

a first integrated circuit supported by the first card;

a second card in a second one of the connectors;

a second integrated circuit supported by the second card;

a power supply in the housing;

conductors coupling the power supply to the first integrated circuit via the first connector, the conductors including circuit traces on the first card;

conductors coupling the power supply to the second integrated circuit via the second connector, the conductors including circuit traces on the second card; and

an optical interconnect coupling the first integrated circuit to the second integrated circuit for data communications, the optical interconnect being within the housing, in use, wherein the optical interconnect does not pass through the connectors.

20. A computer in accordance with claim 19, and further comprising a third card in a third one of the connectors, a co-processor supported by the third card, and an optical interconnect coupling the co-processor to the processor wherein the first integrated circuit comprises a processor, and wherein the second integrated circuit comprises a memory.

21. A computer in accordance with claim 20 and further comprising conductors coupling the power supply to the co-processor via the third connector, the conductors including circuit traces on the third card.

22. A computer in accordance with claim 20 wherein the co-processor is a math co-processor.

23. A computer in accordance with claim 20 and further including an electronic device in the housing capable of generating electromagnetic interference, and wherein the optical interconnect shields communications between the processor and the memory from the electromagnetic interference.

24. A method of assembling a system, the method comprising:

supporting a circuit board in a housing;

supporting a plurality of slot connectors on the circuit board;

mounting a first circuit component on a first card;

inserting the first card into a first one of the slot connectors;

mounting a second circuit component on a second card;

inserting the second card into a second one of the slot connectors; and

flexibly optically coupling the first card to the second card for optical communications between the first circuit component and the second circuit component, using a first optical connector supported by the first card and completely movable with the first card, a second optical connector supported by the second card and completely movable with the second card, and an optical cable coupled between the first and second optical connectors, whereby the flexible optical interconnect does not pass through the slot connectors so that interference that could otherwise be caused by signals to and from the first circuit component is impeded.

25. A method of assembling a system in accordance with claim 24 wherein optically coupling the first card to the second card comprises using a fiber optic cable.

26. A method of assembling a system in accordance with claim 24 wherein optically coupling the first card to the second card comprises supporting an optical connector on the first card to convert between electrical signals and optical signals, and forming circuit traces on the first card to couple the optical connector to the first circuit component.

27. A method of assembling a system in accordance with claim 24 wherein optically coupling the first card to the second card comprises supporting an optical connector on the second card to convert between electrical signals and optical signals, and forming circuit traces on the second card to couple the optical connector to the second circuit component.

28. A method of assembling a system in accordance with claim 24 wherein optically coupling the first card to the second card comprises supporting an optical connector on the first card to convert between electrical signals and optical signals, forming circuit traces on the first card to couple the optical connector to the first circuit component, supporting an optical connector on the second card to convert between electrical signals and optical signals, and forming circuit traces on the second card to couple the optical connector to the second circuit component.

29. A method of assembling a system in accordance with claim 24 wherein mounting the second circuit component comprises mounting a DRAM on the first card.

30. A method of assembling a system in accordance with claim 24 wherein mounting the second circuit component comprises mounting a synchronous link type DRAM on the first card.

31. A method comprising:

supporting a circuit board in a housing;

supporting a plurality of slot connectors on the circuit board;

supporting a processor on a first card having an edge connector;

inserting the edge connector of the first card into a first one of the slot connectors to support the first card from the circuit board;

providing a second card having an edge connector configured for sliding receipt in a second one of the slot connectors;

supporting a synchronous link DRAM memory on a second card having an edge connector;

inserting the edge connector of the second card into a second one of the slot connectors to support the second card from the circuit board;

supporting a power supply in the housing;

coupling the power supply to the processor via the first slot connector, the coupling including using circuit traces on the first card extending from the edge connector of the first card toward the processor;

coupling the power supply to the memory via the second slot connector, the coupling including using circuit traces on the second card extending from the edge connector of the second card toward the memory; and

optically coupling the processor to the memory for data communications using an optical interconnect within the housing, wherein the optical interconnect does not pass through the slot connectors.

32. A method in accordance with claim 31 and further comprising supporting a co-processor on a third card having an edge connector, and optically coupling the co-processor to the processor.

33. A method in accordance with claim 32 and further comprising coupling the power supply to the co-processor via the third slot connector, the coupling comprising using circuit traces on the third card extending from the edge connector of the third card toward the co-processor.

34. A method in accordance with claim 32 wherein supporting a co-processor comprises supporting a math co-processor on the third card.

35. A method comprising:

supporting a circuit board in a housing;

supporting a plurality of slot connectors on the circuit board;

supporting a first integrated circuit on a first card having an edge connector;

inserting the edge connector of the first card into a first one of the slot connectors to support the first card from the circuit board;

providing a second card having an edge connector configured for sliding receipt in a second one of the slot connectors;

supporting a second integrated circuit on a second card having an edge connector;

inserting the edge connector of the second card into a second one of the slot connectors to support the second card from the circuit board;

supporting a power supply in the housing;

coupling the power supply to the first integrated circuit via the first slot connector, the coupling including using circuit traces on the first card extending from the edge connector of the first card toward the first integrated circuit;

coupling the power supply to the second integrated circuit via the second slot connector, the coupling including using circuit traces on the second card extending from the edge connector of the second card toward the second integrated circuit; and

optically coupling the first integrated circuit to the second integrated circuit for data communications using an optical interconnect within the housing, wherein the optical interconnect does not pass through the slot connectors.

36. A method in accordance with claim 35 and further comprising supporting a co-processor on a third card having an edge connector, and optically coupling the co-processor to the processor, wherein the first integrated circuit comprises a processor, and wherein the second integrated circuit comprises a memory.

37. A method in accordance with claim 36 and further comprising coupling the power supply to the co-processor via the third slot connector, the coupling comprising using circuit traces on the third card extending from the edge connector of the third card toward the co-processor.

38. A method in accordance with claim 36 wherein supporting a co-processor comprises supporting a math co-processor on the third card.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

Application Serial No. 10/799,244
Confirmation No.....8217
Filing Date.....March 12, 2004
Inventors.....Warren M. Farnworth et al.
Assignee.....Micron Technology, Inc.
Group Art Unit 2116
Examiner.....Tse W. Chen
Attorney's Docket No.....MI22-2488
Customer No.....021567
Title: Computer Including Installable and Removable Cards, Optical Interconnect Between Cards, and Method of Assembling a Computer

Evidence Appendix

There is no evidence submitted pursuant to §§1.130, 1.131, or 1.132 of this title or any other evidence entered by the Examiner and relied upon by Appellant in this Appeal.

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Related Proceedings Appendix

There are no known decisions rendered by a court or the Board in any proceeding identified pursuant to paragraph (c)(1)(ii) of 37 CFR 41.37.